AMENDED CLAIM SET

1. (currently amended) In a processor, an apparatus for issuing instructions, wherein said processor has a memory, a decoding unit, and an execution unit, said apparatus comprising:

a classification logic adapted for prioritizing instructions in relation to one another and sorting said instructions in a number of priority categories, wherein said instructions come from said memory and are being decoded in said decoding unit prior of reaching said classification logic, and wherein said instructions sorted in said number of priority categories by said classification logic comprise cloned instructions;

a plurality of instruction queues, wherein said queues contain said instructions in decoded form, wherein said plurality of said queues matches said number of said priority categories, and wherein each of said queues adapted to receive only one of said priority categories of said instructions from said classification logic, whereby said queues having same priority categories as said instructions, and wherein said cloned instructions and corresponding unmodified instructions from which said cloned instructions have been derived are found in different ones of said queues; and

an issue logic to dispatch said instructions for execution in said execution unit of said processor, wherein said issue logic is operably coupled to said plurality of instruction queues and is selecting from which of said queues to dispatch said instructions for execution, wherein said issue logic has been designed to be cognizant of said priority

categories of said queues.

2. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus forms part of an in-order instruction issue processor architecture.

3. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus forms part of an out-of-order instruction issue processor architecture.

4. (original) The apparatus for issuing instructions of claim 1, wherein said plurality of instruction queues consist of two queues, a high priority queue and a low priority queue.

5. (canceled)

6. (canceled)

7. (original) The apparatus for issuing instructions of claim 1, wherein said prioritizing of said instructions is based on said instructions being scalar instructions or vector instructions.

8. (original) The apparatus for issuing instructions of claim 1, wherein said prioritizing of said instructions is based on a conditionality of branching.

9. (original) The apparatus for issuing instructions of claim 1, wherein said prioritizing of said instructions is based on a probability for memory miss.

10. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus is designed for prioritizing and issuing said instructions in a static manner.

11. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus is designed for prioritizing and issuing said instructions in a dynamic manner.

12. (original) The apparatus for issuing instructions of claim 1, wherein said apparatus further comprising a predictor unit operably coupled to said classification logic, wherein said predictor unit identifies performance-critical instructions.

13. (original) The apparatus for issuing instructions of claim 1, wherein said classification logic further adapted for receiving preannotated instructions, wherein said instructions have been preannotated during compilation time and said preannotations indicate said priority categories.

14. (currently amended) In a processor, a method for issuing instructions, comprising the steps of:

decoding instruction coming from a memory in a decoding unit and passing said

instructions to a classification logic;

prioritizing said instructions in relation to one another in said classification logic;

sorting said instructions in a number of priority categories by said classification logic, wherein said instructions comprise cloned instructions;

providing a plurality of instruction queues for containing said instructions in decoded form, wherein said plurality of said queues matching said number of said priority categories, and wherein each of said queues adapted to receive only one of said priority categories of said instructions from said classification logic, whereby said queues having same priority categories as said instructions, wherein said cloned instructions and corresponding unmodified instructions from which said cloned instructions have been derived are being sorted into different ones of said queues; and

selecting from which of said queues to dispatch said instructions for execution in an execution unit of said processor by an issue logic, wherein said issue logic is operably coupled to said plurality of instruction queues and, wherein said issue logic has been designed to be cognizant of said priority categories of said queues.

15. (original) The method for issuing instructions of claim 14, wherein said method is being executed in an in-order instruction issue processor architecture.

16. (original) The method for issuing instructions of claim 14, wherein said method is being executed in an out-of-order instruction issue processor architecture.

17. (original) The method for issuing instructions of claim 14, wherein said step of providing a plurality of instruction queues consist of providing two queues, a high priority queue and a low priority queue.

18. (canceled)

19. (canceled)

20. (original) The method for issuing instructions of claim 14, wherein said prioritizing step is performed based on said instructions being scalar instructions or vector instructions.

21. (original) The method for issuing instructions of claim 14, wherein said prioritizing step is performed based on a conditionality of branching.

22. (original) The method for issuing instructions of claim 14, wherein said prioritizing step is performed based on a probability for memory miss.

23. (original) The method for issuing instructions of claim 14, wherein said prioritizing and selecting steps are performed statically.

24. (original) The method for issuing instructions of claim 14, wherein said prioritizing and selecting steps are performed dynamically.

25. (original) The method for issuing instructions of claim 14, further comprises identifying performance-critical instructions with a predictor unit, wherein said predictor unit is operably coupled to said classification logic.

26. (original) The method for issuing instructions of claim 14, further comprising the step of adapting said classification logic to receive preannotated instructions, wherein said instructions have been preannotated during compilation time and said preannotations indicate said priority categories.

27. (original) A program storage device, readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for issuing instructions as recited in claim 14.

CLOSING STATEMENT

Applicant respectfully submits that as expressed in this amendment the claims now put forward only allowed subject matter.

Applicant submits that this application is now in condition for allowance, which action is respectfully requested.

Respectfully,

George Sai-Halasz, PhD
Registration # 45,430

145 Fernwood Drive
E. Greenwich, RI 02818.
401-885-8032 (Fax 401-885-1046)
E-MAIL - patents@computer.org

Cust. No.: **24299**